ABSTRACT OF THE DISCLOSURE

Method and apparatus for increasing the number of real memory addresses accessible through a translational look-aside buffer (TLB) by a multi thread CPU. The buffer entries include a virtual address, a real address and a special mode bit indicating whether the address represents one of a plurality of threads being processed by the CPU. If the special mode bit is set, the real address associated with the virtual address higher order bits are concatenated with the thread identification number being processed to obtain a real address. Buffer entries containing no special mode bit, or special mode bit set to 0, are processed by using the full length of the real address associated with the virtual address stored in the look-aside buffer (TLB).